EE 330
Lecture 12

Back-End Processing

Semiconductor Processes

Devices in Semiconductor Processes

- Resistors
- Diodes
- Capacitors
- MOSFET
- BJT

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Exam 1 Schedule

Exam 1 will be given on Friday September 23

Format: Open-Book, Open Notes

Exam will be posted at 9:00 a.m. on the class WEB site and will be due at 1:00 p.m. as a .pdf upload on CANVAS

It will be structured to be a 50-minute closed-book closed-notes exam but administered as an open-book, open-notes exam with a 4 hour open interval so reserving the normal lecture period for taking the exam should provide adequate time

Honor System Expected

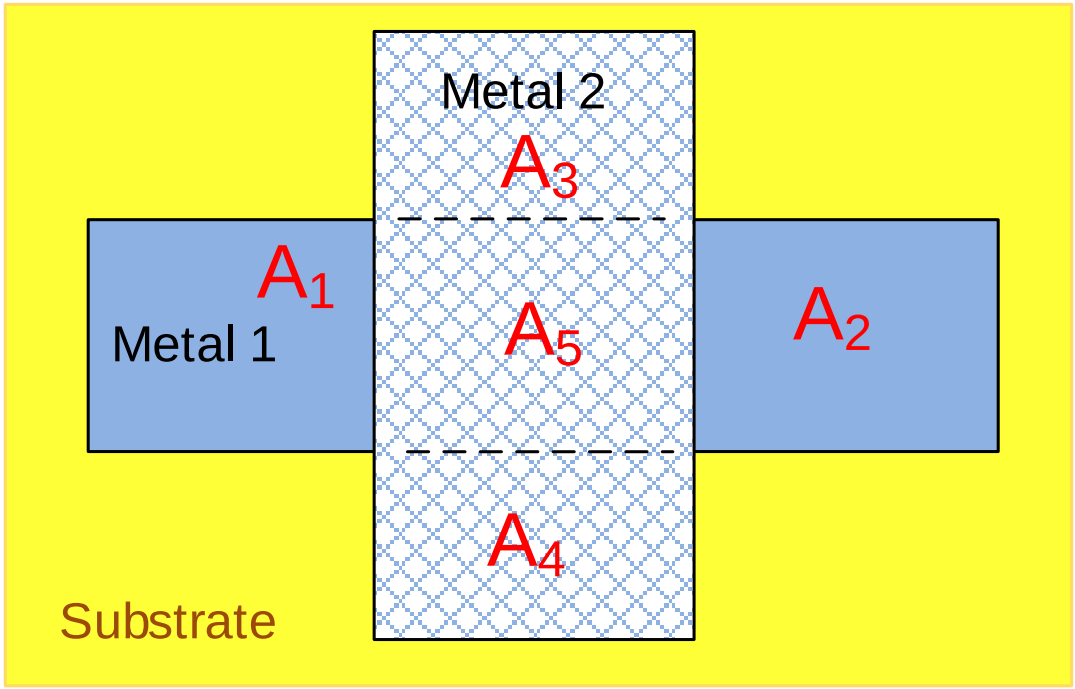
It is expected that this exam be an individual effort and that students should not have input in **any form** from **anyone else** during the 4-hour open interval of the exam except from the course instructor who will be responding to email messages from 11:00 a.m. to 1:00 p.m. on the date of the exam.

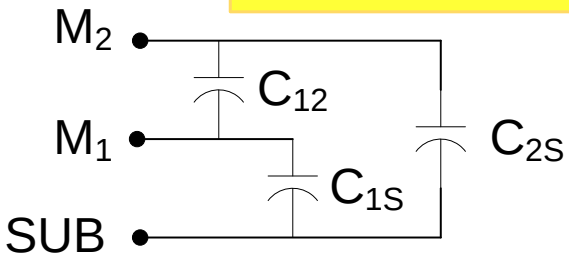
Special Accommodations

For anyone with approved special accommodations, the 4-hour open interval should cover extra time allocations but if for any reason this does not meet special accommodation expectations, please contact the instructor by Monday Sept. 14 if alternative accommodations are requested.

Review from Last Lecture

Capacitance in Interconnects





$$C_{12}=CD_{12}\,A_5$$

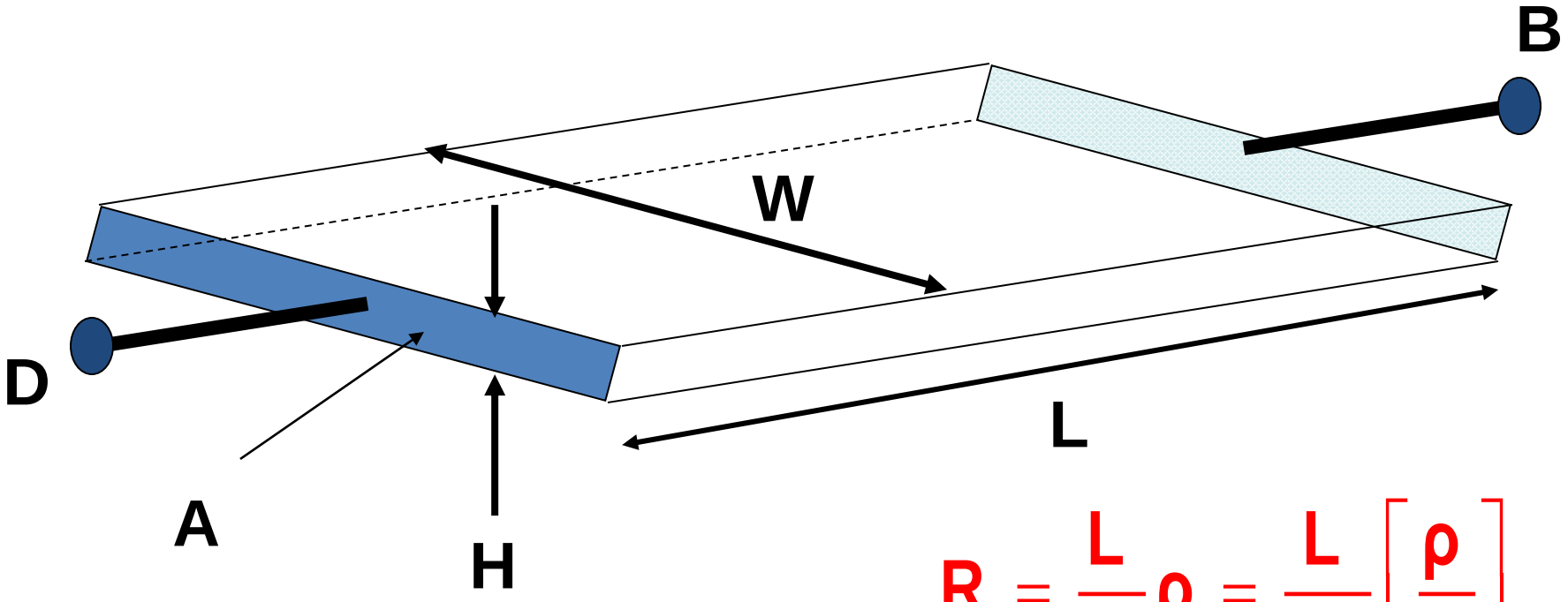
$$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Equivalent Circuit

Review from Last Lecture

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

Review from Last Lecture

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

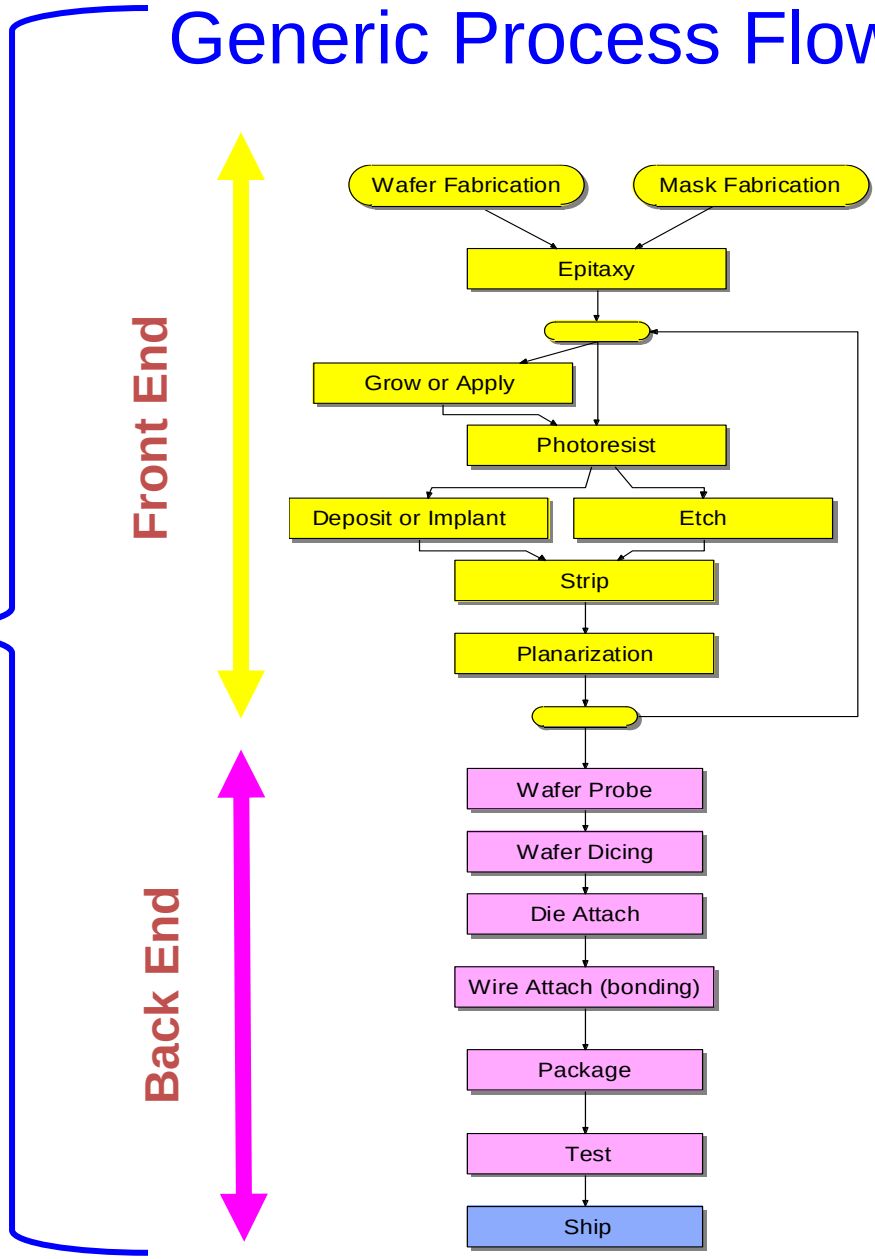
CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

Back End Processing

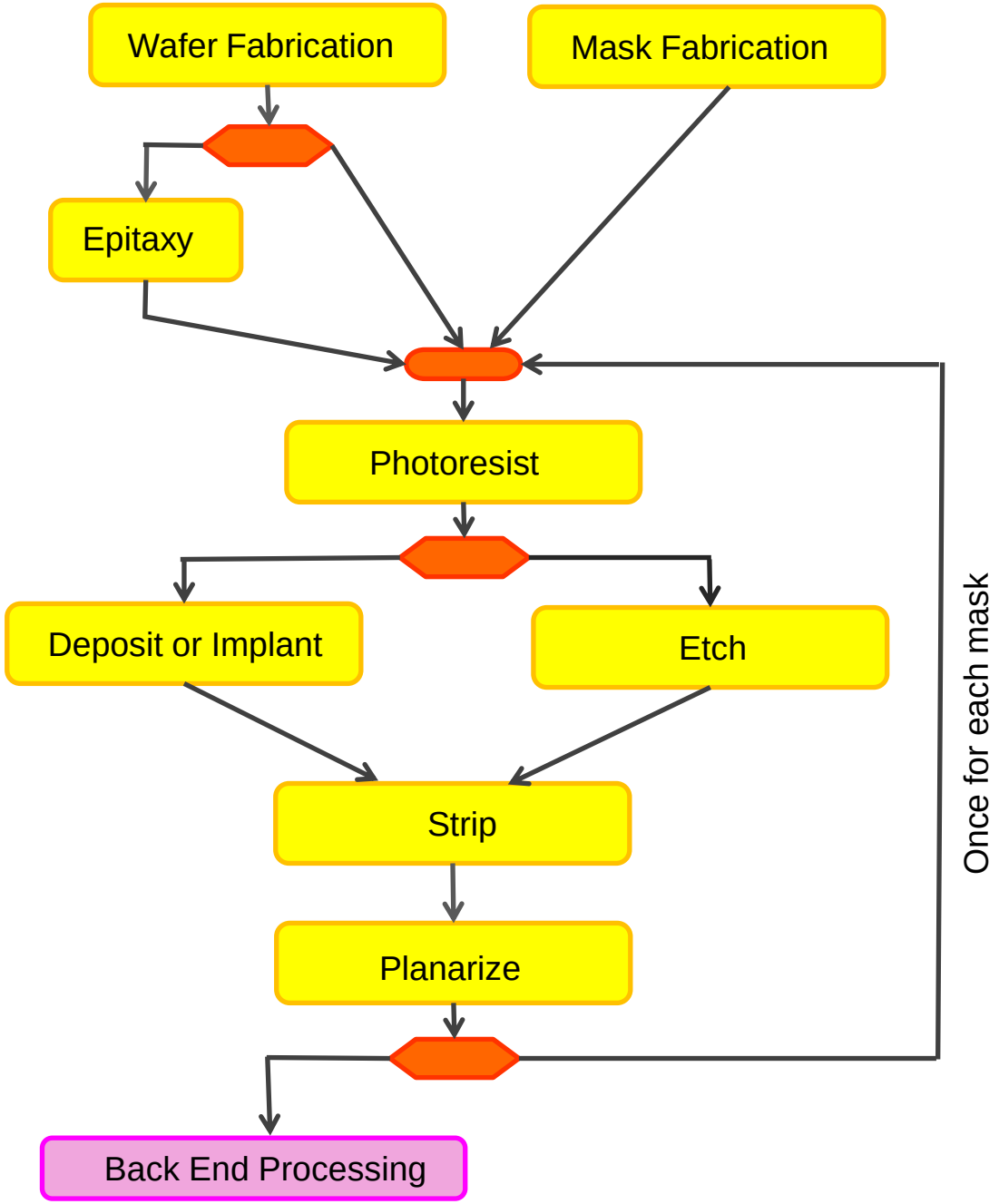
Recall:

Generic Process Flow



Front End Process Integration for Fabrication of ICs

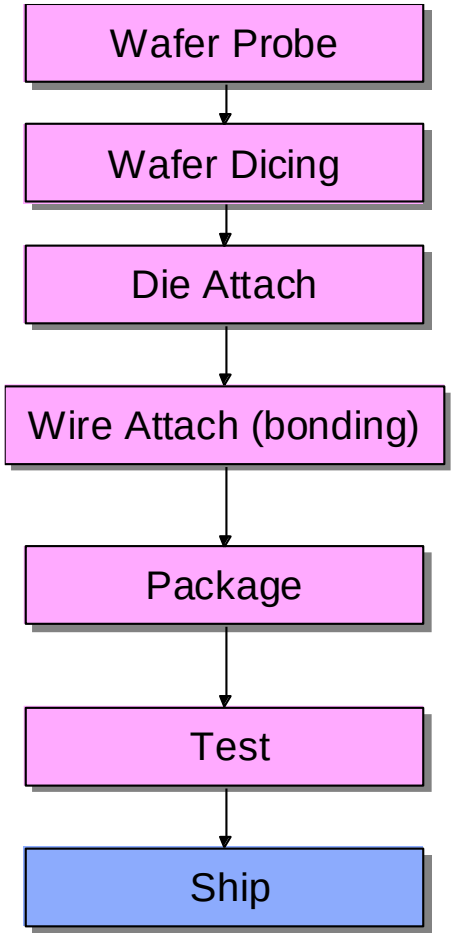
Recall:



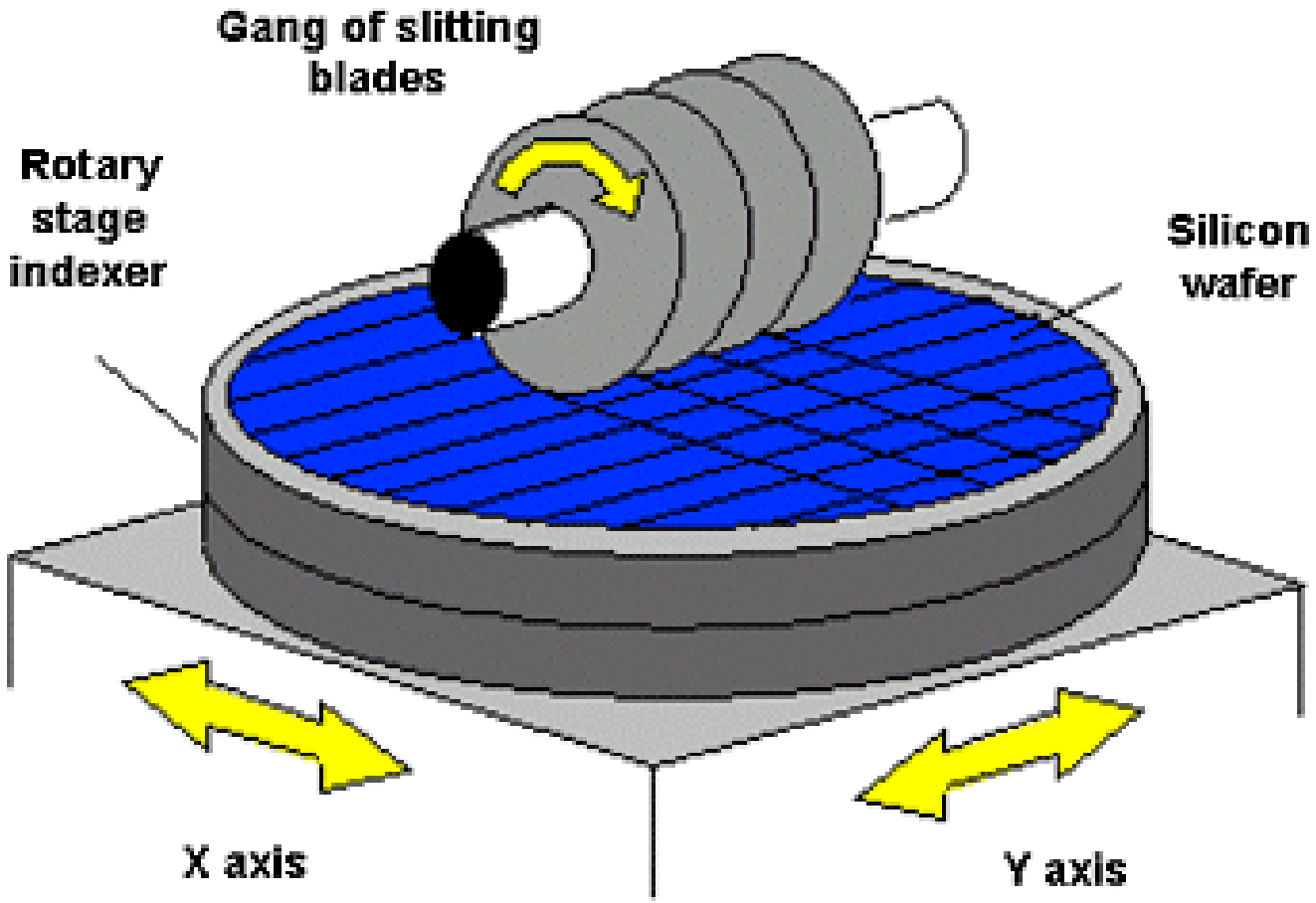
Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary

Back-End Process Flow



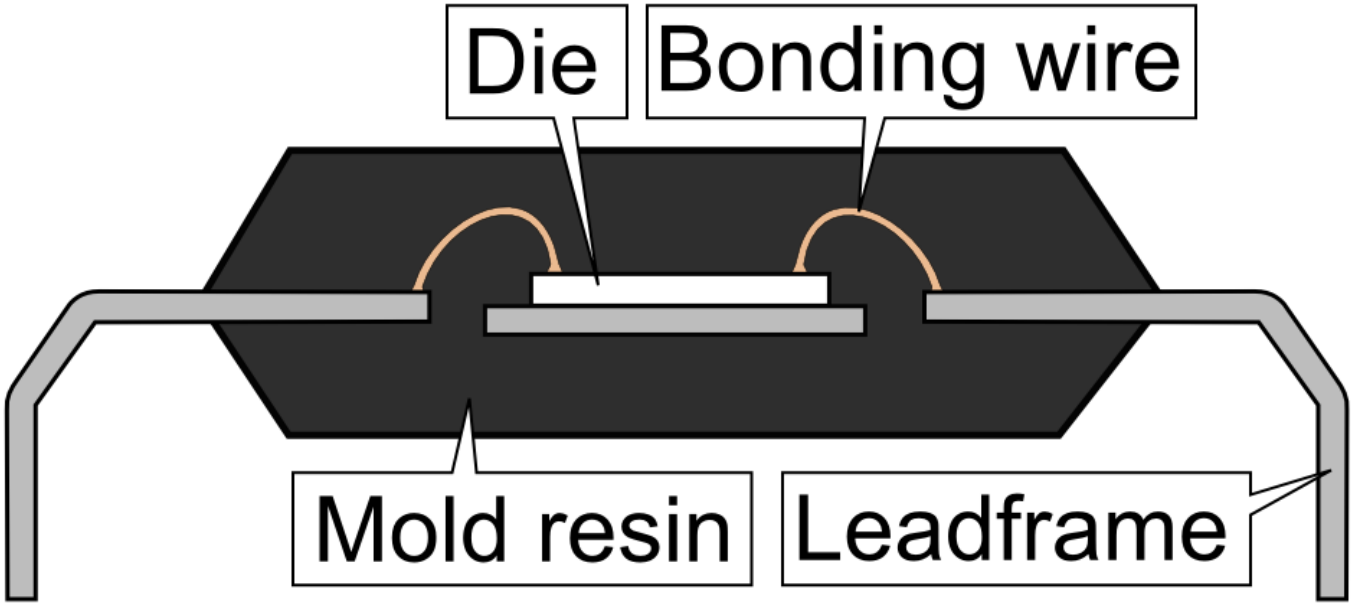
Wafer Dicing



www.renishaw.com

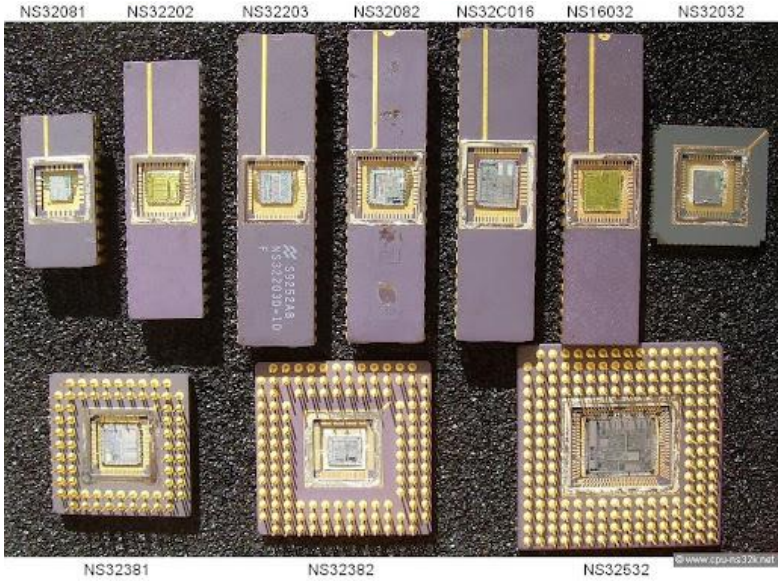
Die Attach

DIP



Die Attach

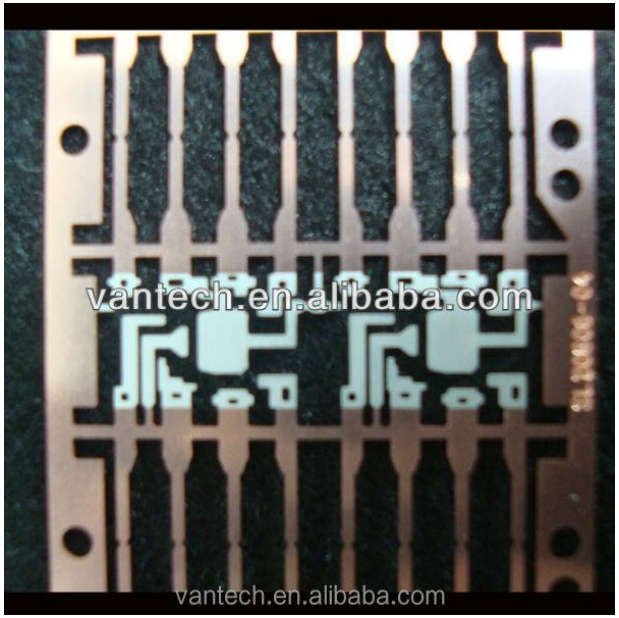
Package

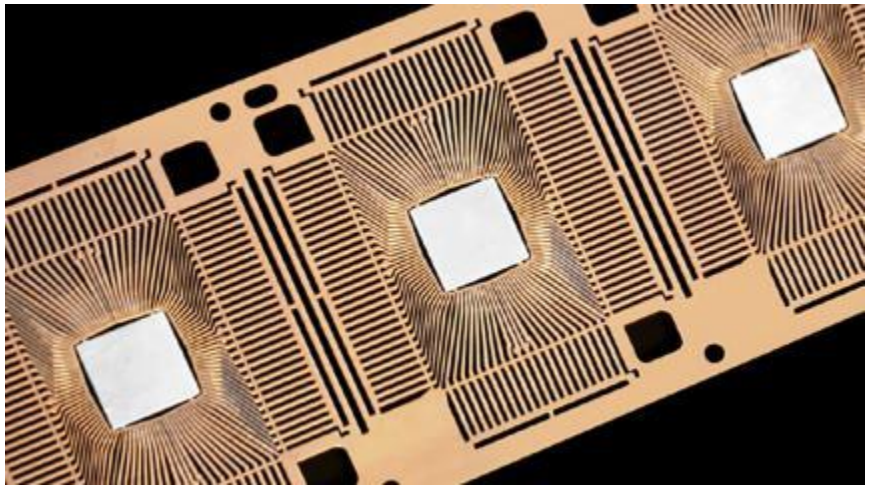


Packaged Die

Old Technology but Good for Illustration

Die Attach





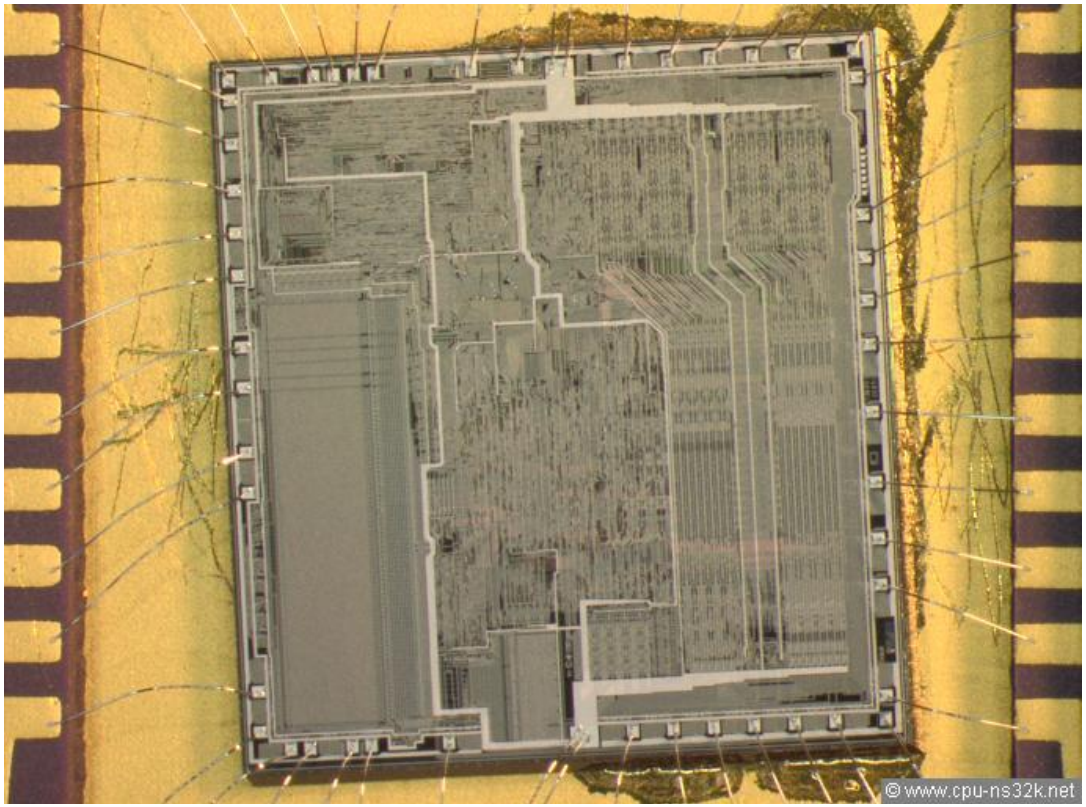
Lead Frame (for injection molded package)

Prior to Die Attachment

Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy

Die Attach

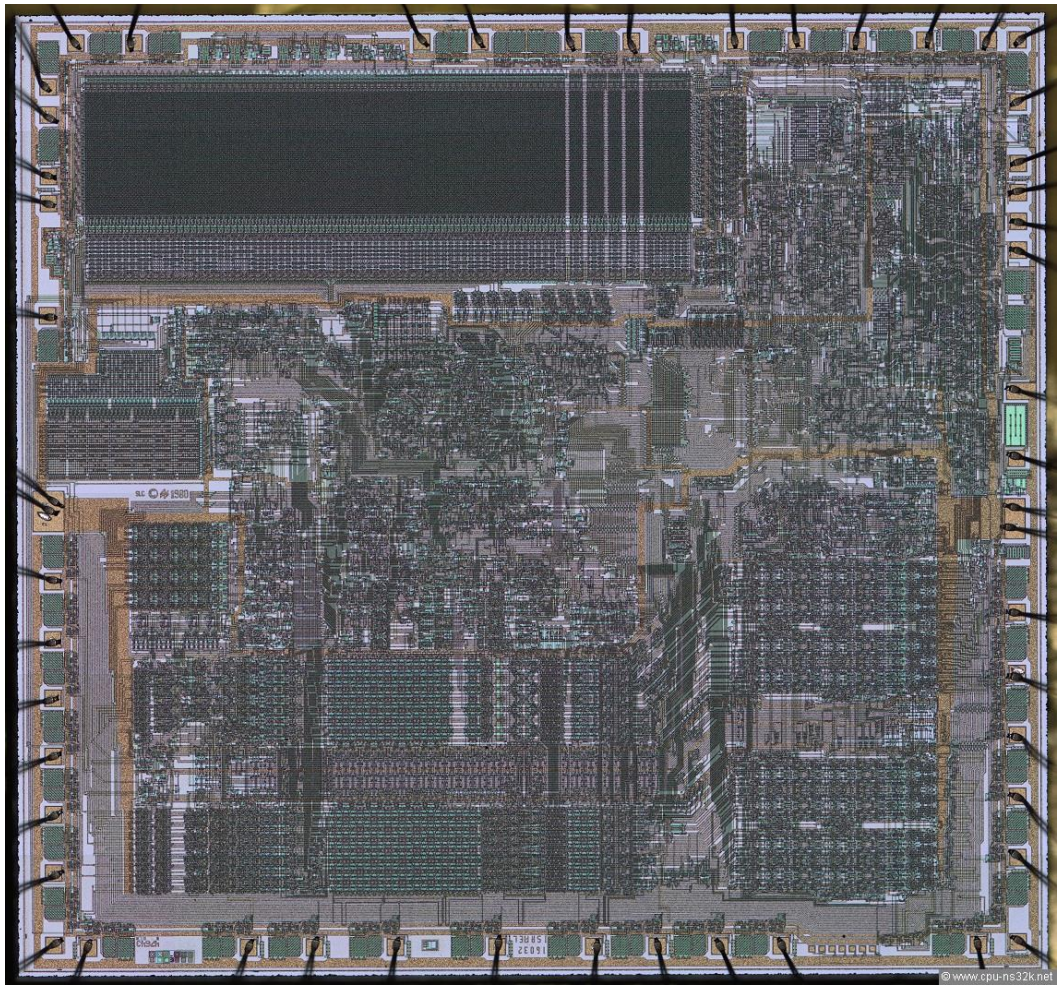


Die attached showing bonding wires and likely solder preform or epoxy residue

Note alignment is not perfect

Die Attach

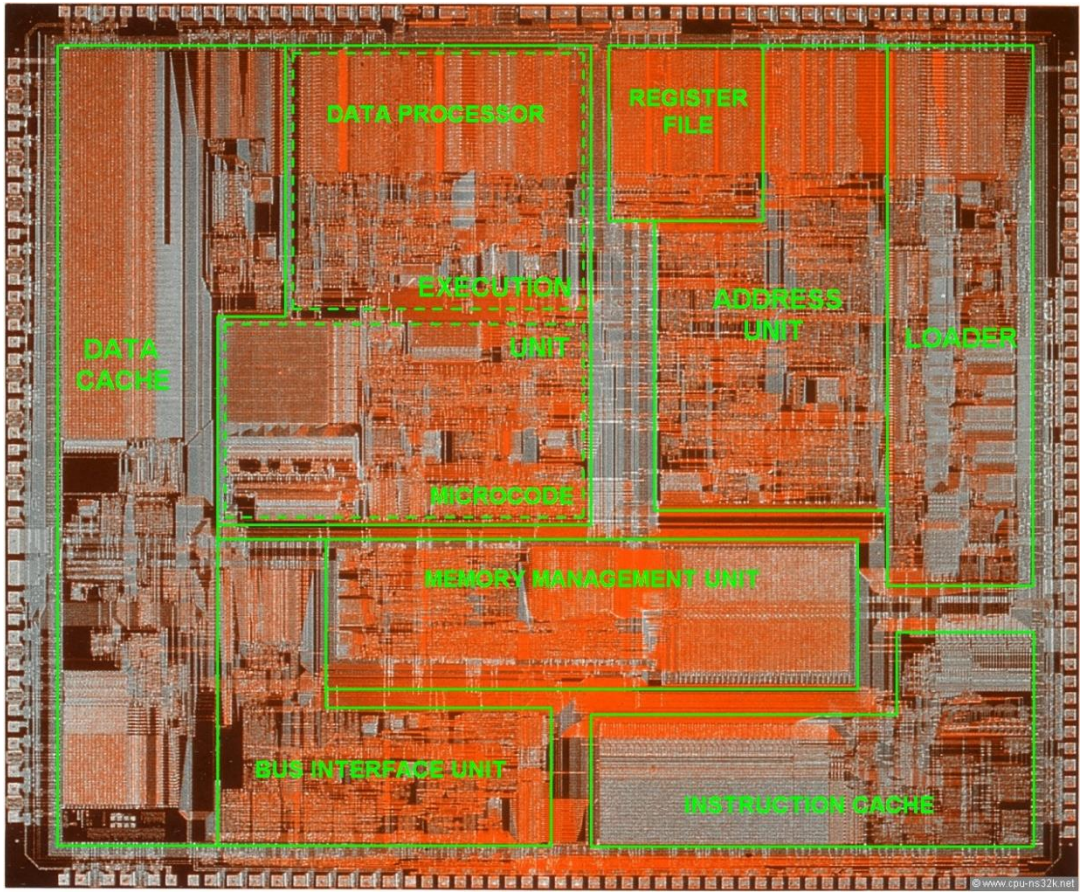
Note double bonding wires



NS16032

http://cpu-ns32k.net/Diephotos.html

Electrical Connections (Bonding)

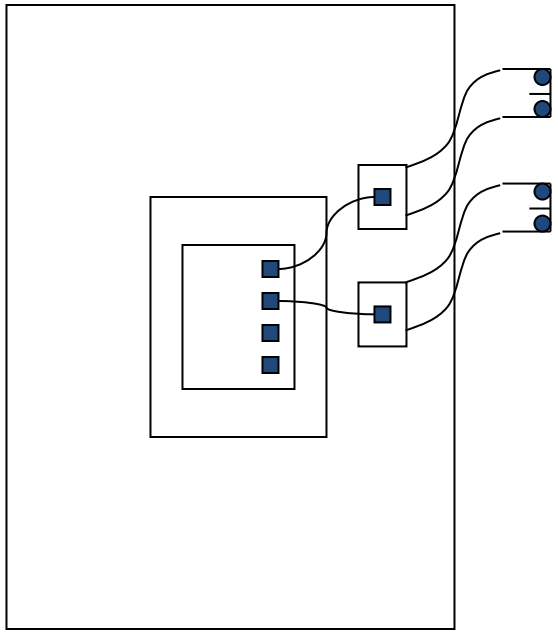


Number of connections can become large (even much larger than shown here)

Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding

Wire Bonding



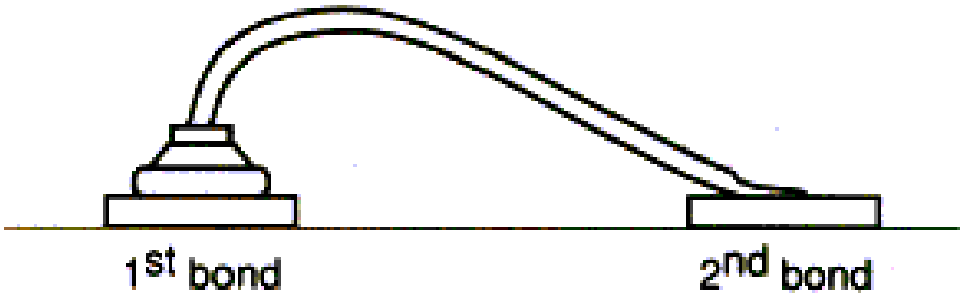
Wire – gold or aluminum
25 μ in diameter

Wire Bonding

Excellent Annimation showing process at :

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf

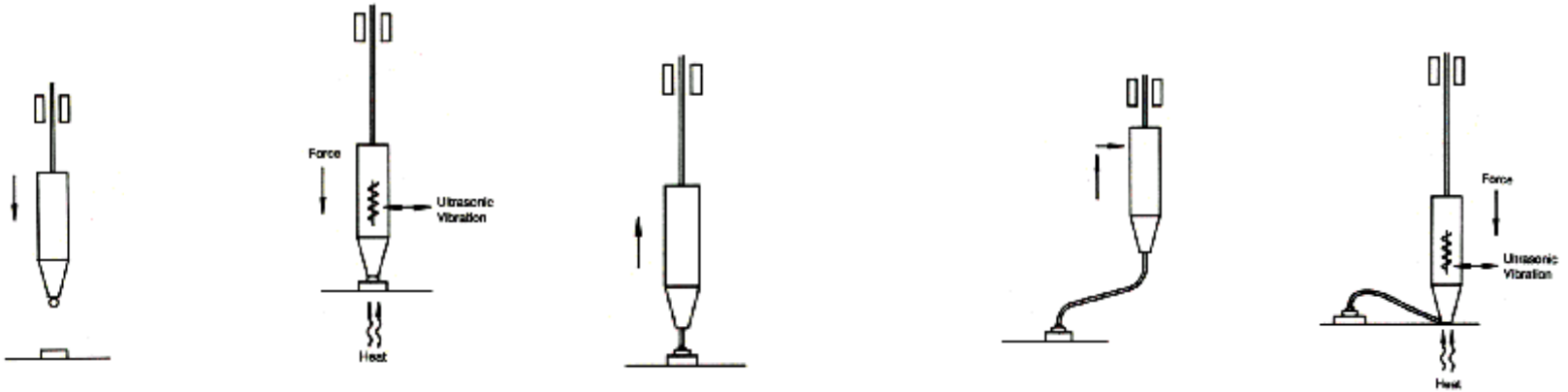
Wire Bonding



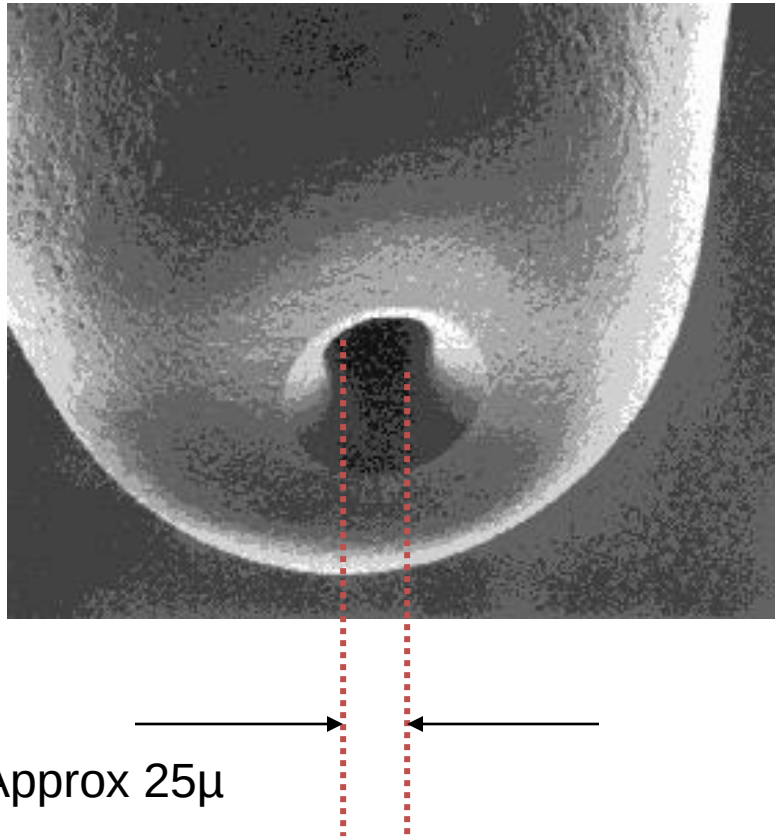
Ball Bond

Wedge Bond

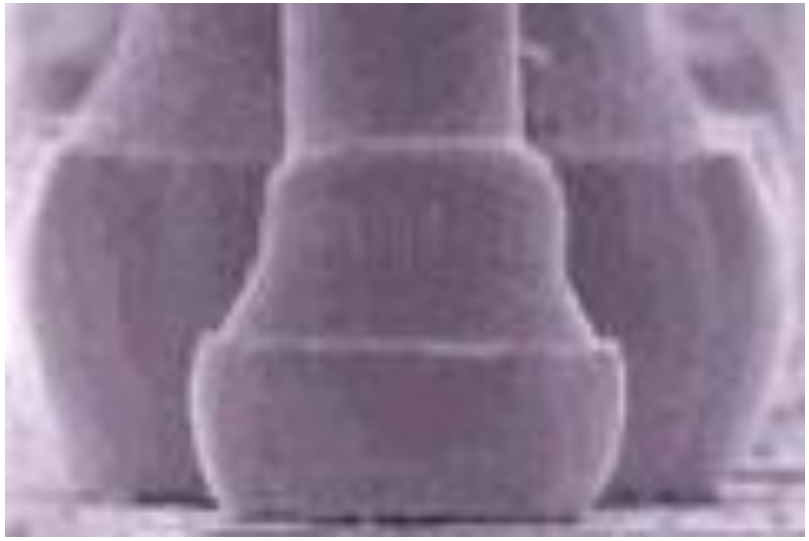
Ball Bonding Steps



Ball Bonding Tip

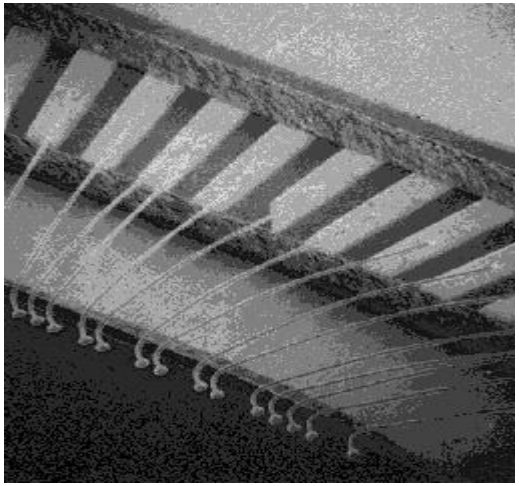


Wire Bonding



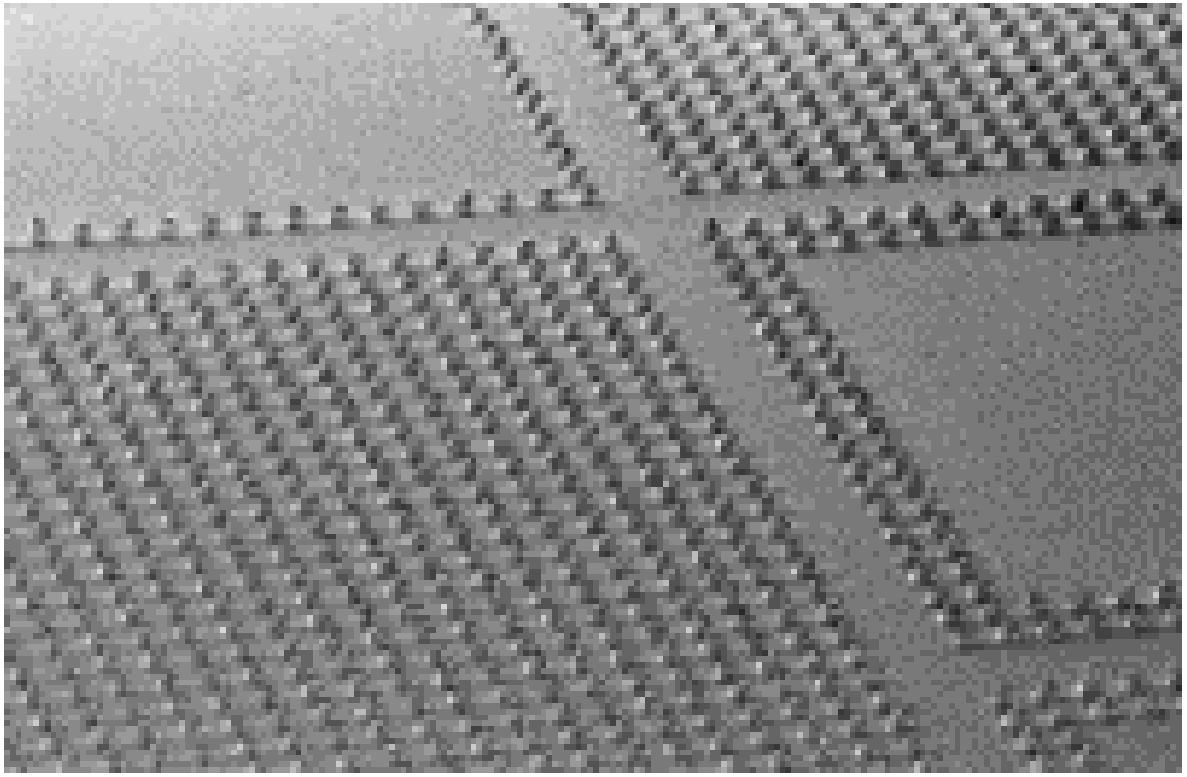
Ball Bond

Termination Bond



Ball Bond Photograph

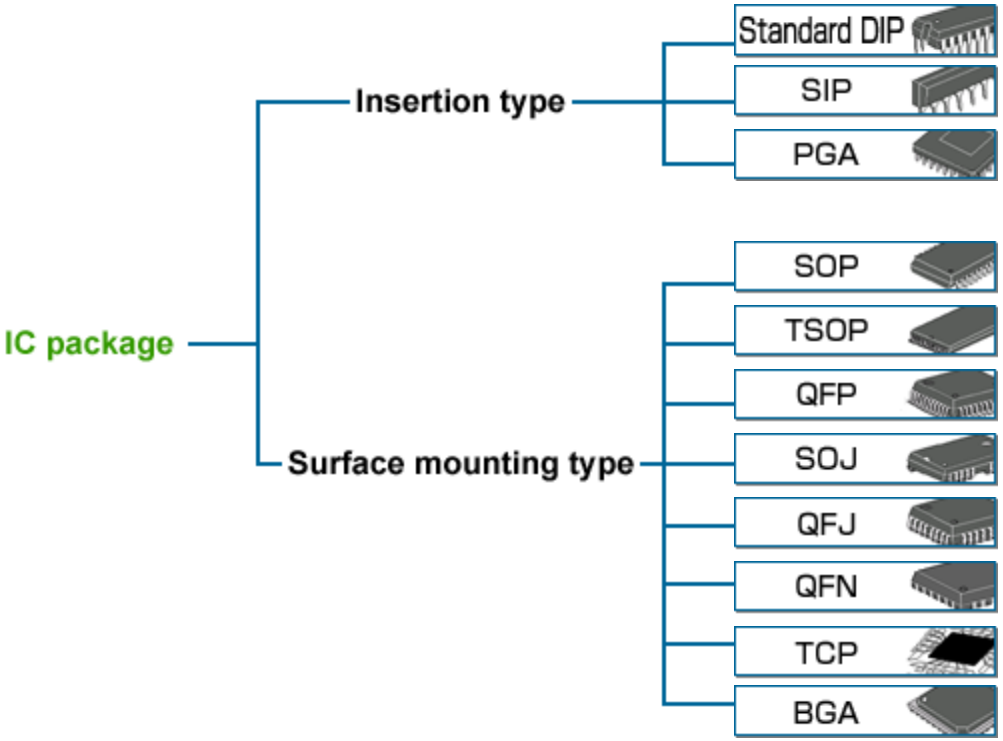
Bump Bonding



Packaging

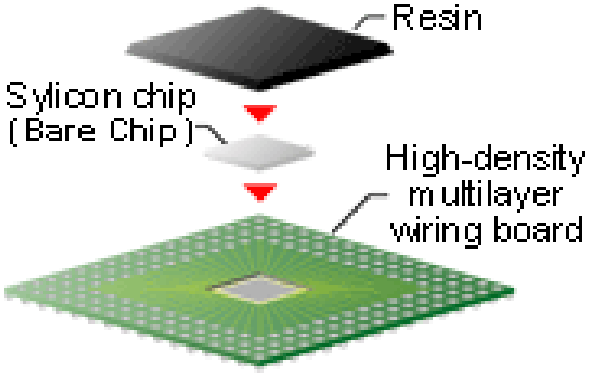
1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

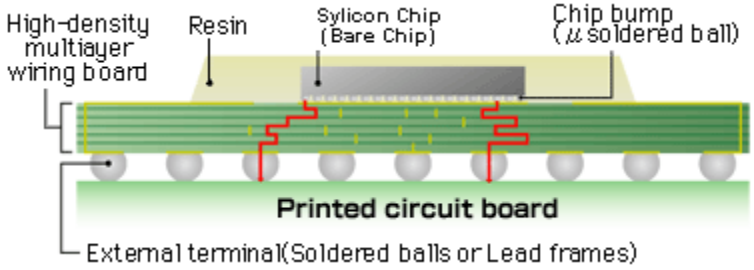
Packaging



www.necel.com

Packaging



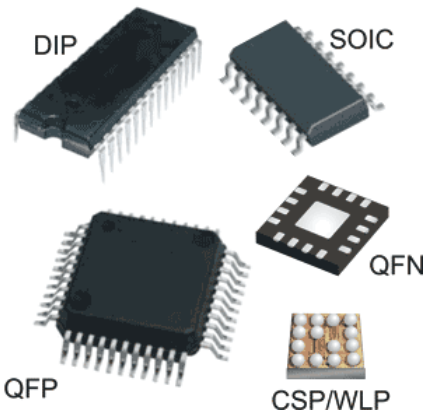


www.necel.com

Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

Name	Pin pitch	Size	Height
DIP or DIL	2.54		
SOIC-16	1.27	3.9 x 10	1.72
SSOP	0.635		
TSSOP54-II	0.8	12.7 x 22.22	~1
PLCC44	1.27		
PQ208[1]	0.50	28 x 28	3.4
TQFP64	0.40	7 x 7	1.0
TQFP144[2]	0.50	20 x 20	1.0
128PQFP	0.50	23.23 x 14.0	3.15



http://www.electroiq.com/index/display/packaging-article-display/234467/articles/advanced-packaging/volume-14/issue-8/features/the-back-end-process/materials-and-methods-for-ic-package-assemblies.htm

From Wikipedia, Sept 20, 2010

http://en.wikipedia.org/wiki/List_of_chip_carriers

Many standard packages available today:

http://www.interfacebus.com/Design_Pack_types.html

BCC: Bump Chip Carrier
BGA: Ball Grid Array; BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, **CPGA Graphic**
CQFP: Ceramic Quad Flat Pack, **CQFP Graphic**
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fpBGA: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) **J-Lead Picture**
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier **LCC Graphic**
LCC: Leaded Chip Carrier **Un-formed LCC Graphic**
LCCC: Leaded Ceramic Chip Carrier;
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, **LGA uP** [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leaded Chip Carrier **LLCC Graphic**
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier

PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack **QFP Graphics**
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SO Flat Pack: Small Outline Flat Pack IC
SOJ: Small-Outline Package [J-Lead]; **J-Lead Picture**
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack

Considerable activity today and for years to come on improving packaging technology

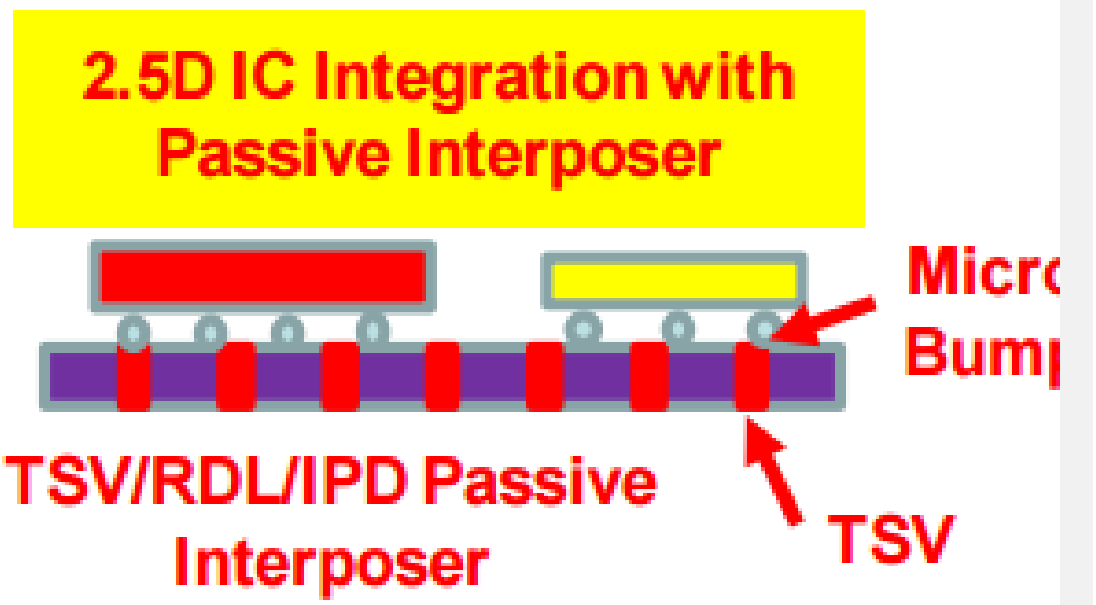
- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained

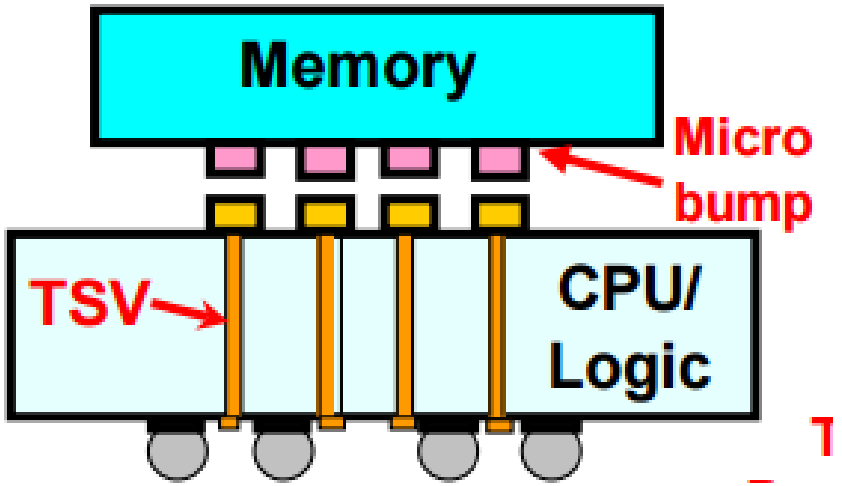
The following few slides come from a John Lau presentation

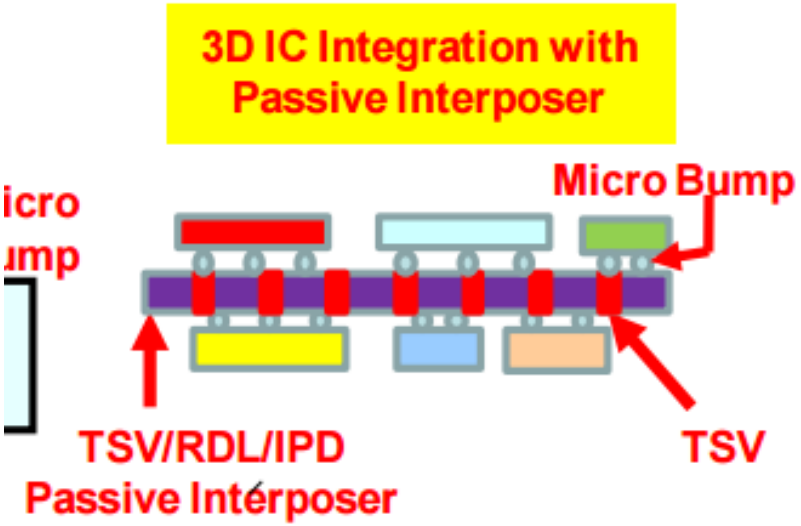
www.sematech.org/meetings/archives/symposia/10187/Session2/04_Lau.pdf

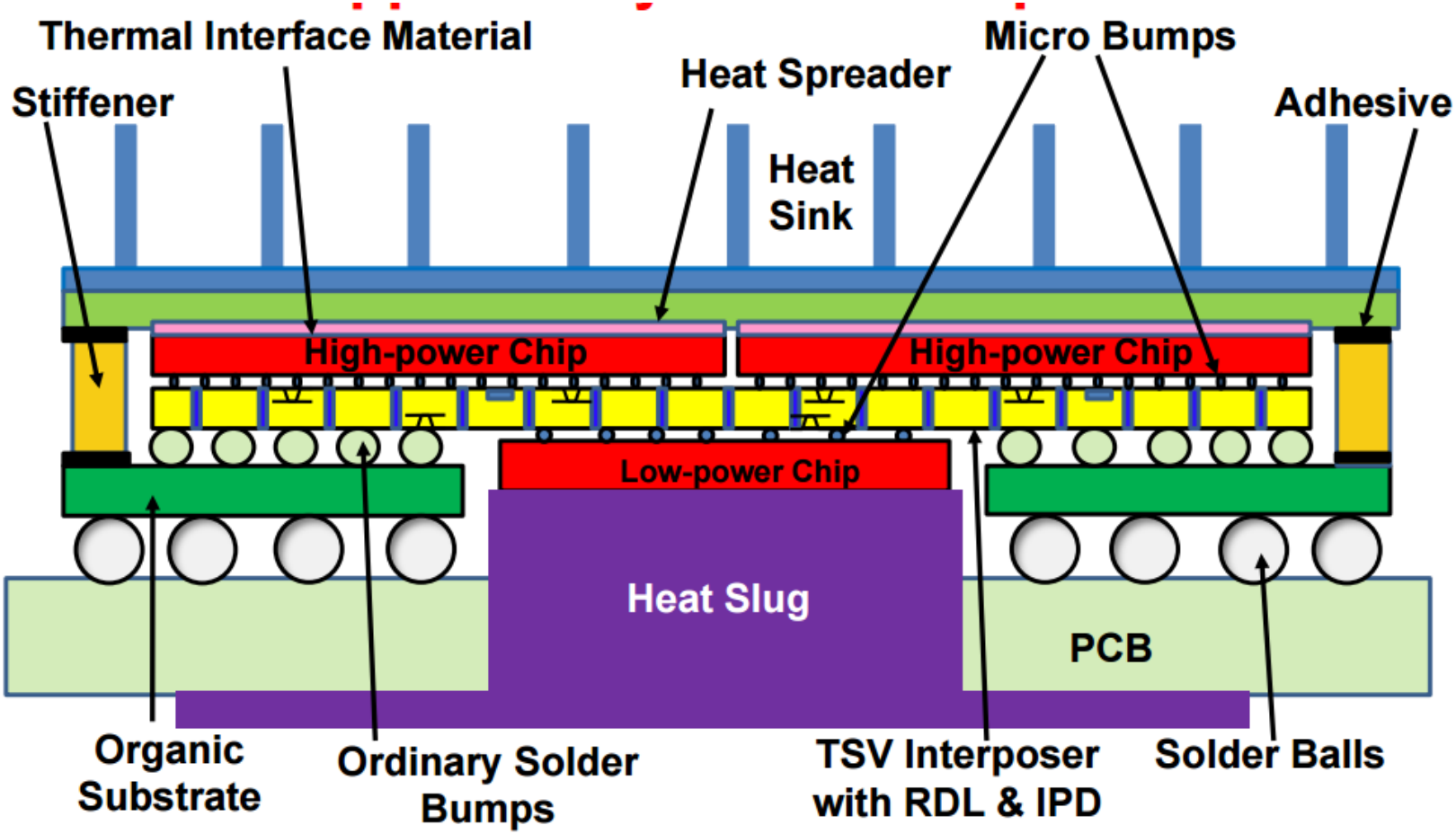
TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration

John H. Lau
Electronics & Optoelectronics Research Laboratories
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan 310, R.O.C.
886-3591-3390, johnlau@itri.org.tw

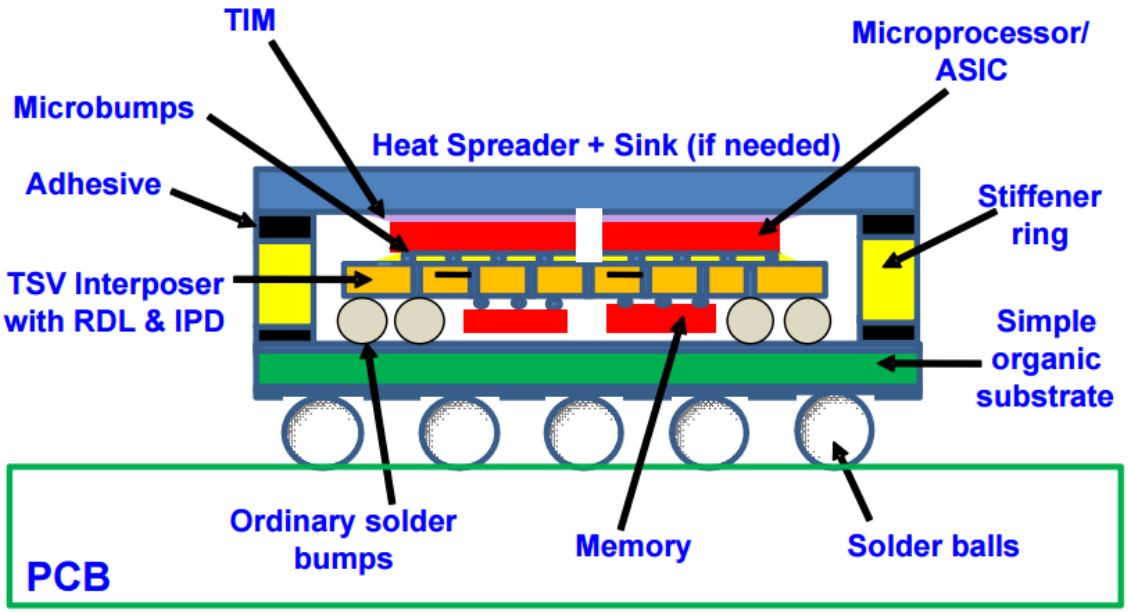

2.5D IC Integration with Passive Interposer
Micro Bump
TSV/RDL/IPD Passive Interposer
TSV


Memory
Micro
bump
TSV
CPU/
Logic


3D IC Integration with
Passive Interposer
Micro Bump
TSV/RDL/IPD
Passive Intérposer
TSV

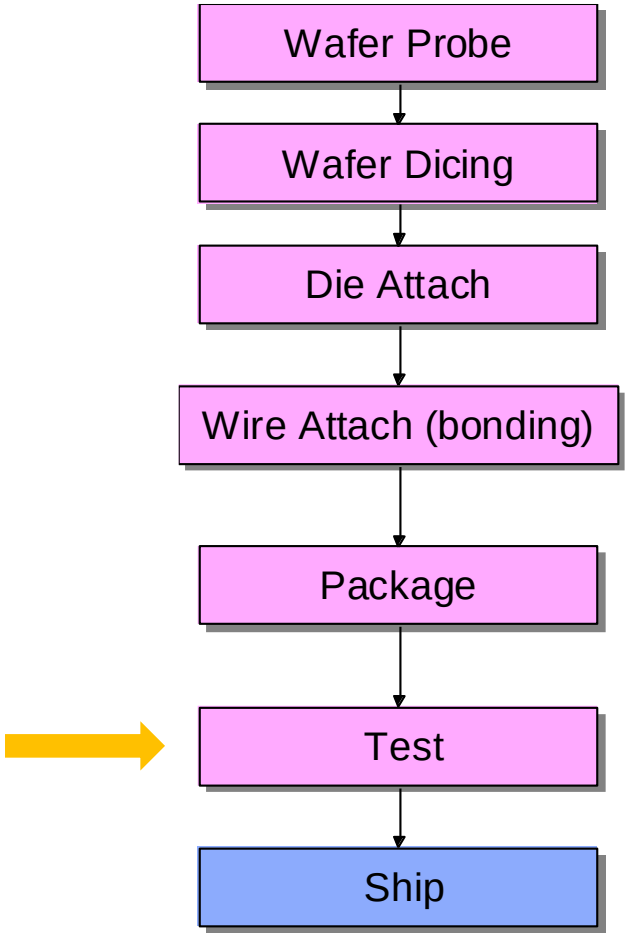

Thermal Interface Material
Stiffener
Heat Spreader
Micro Bumps
Adhesive
Heat
Sink
High-power Chip
High-power Chip
Low-power Chip
Heat Slug
PCB
Organic
Substrate
Ordinary Solder
Bumps
TSV Interposer
with RDL & IPD
Solder Balls

TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side



Special underfills are needed between the Cu -filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.

Back-End Process Flow



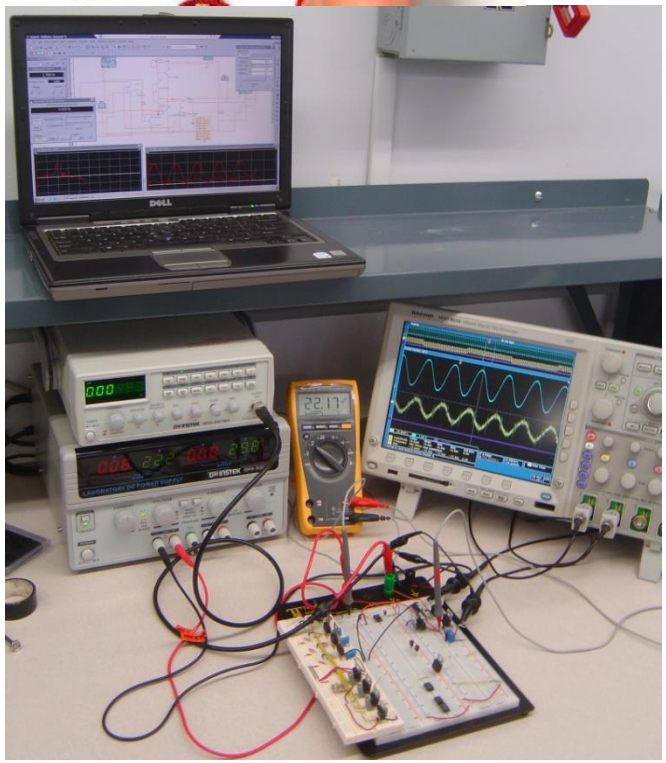
Testing of Integrated Circuits

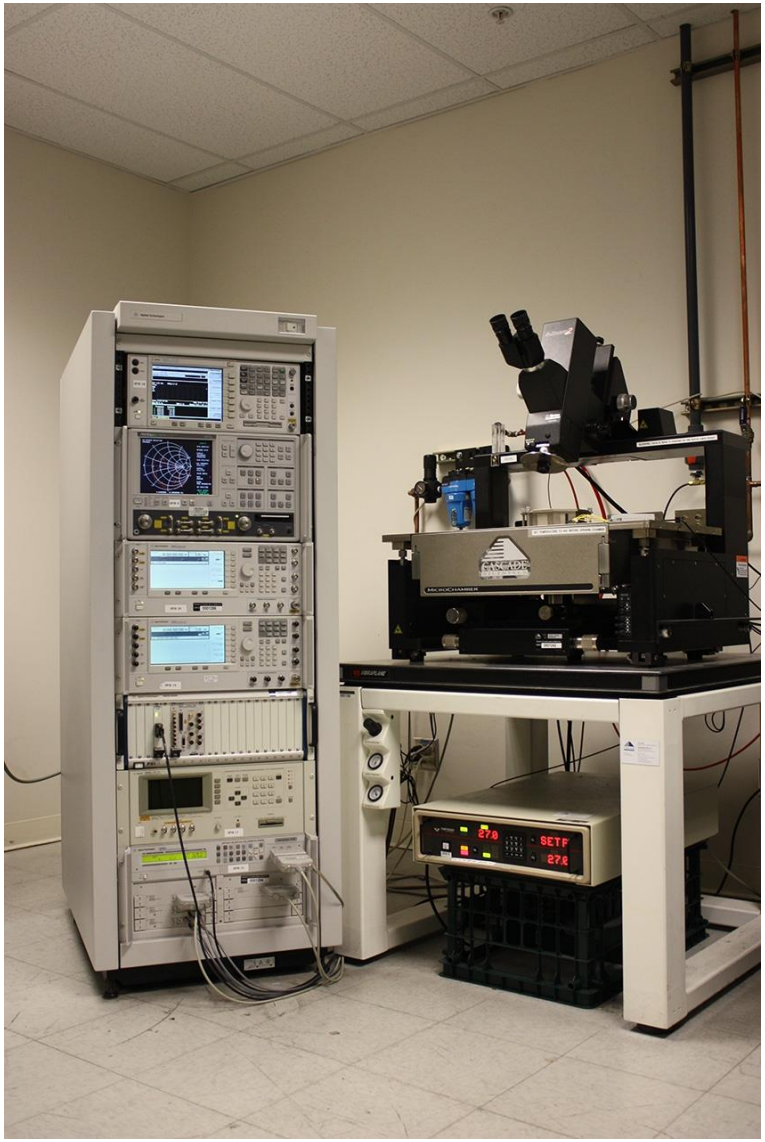
Bench testing used to qualify parts for production

Most integrated circuits are tested twice during production

- Wafer Probe Testing
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts
- Packaged Part Testing
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts

Bench Test Environment



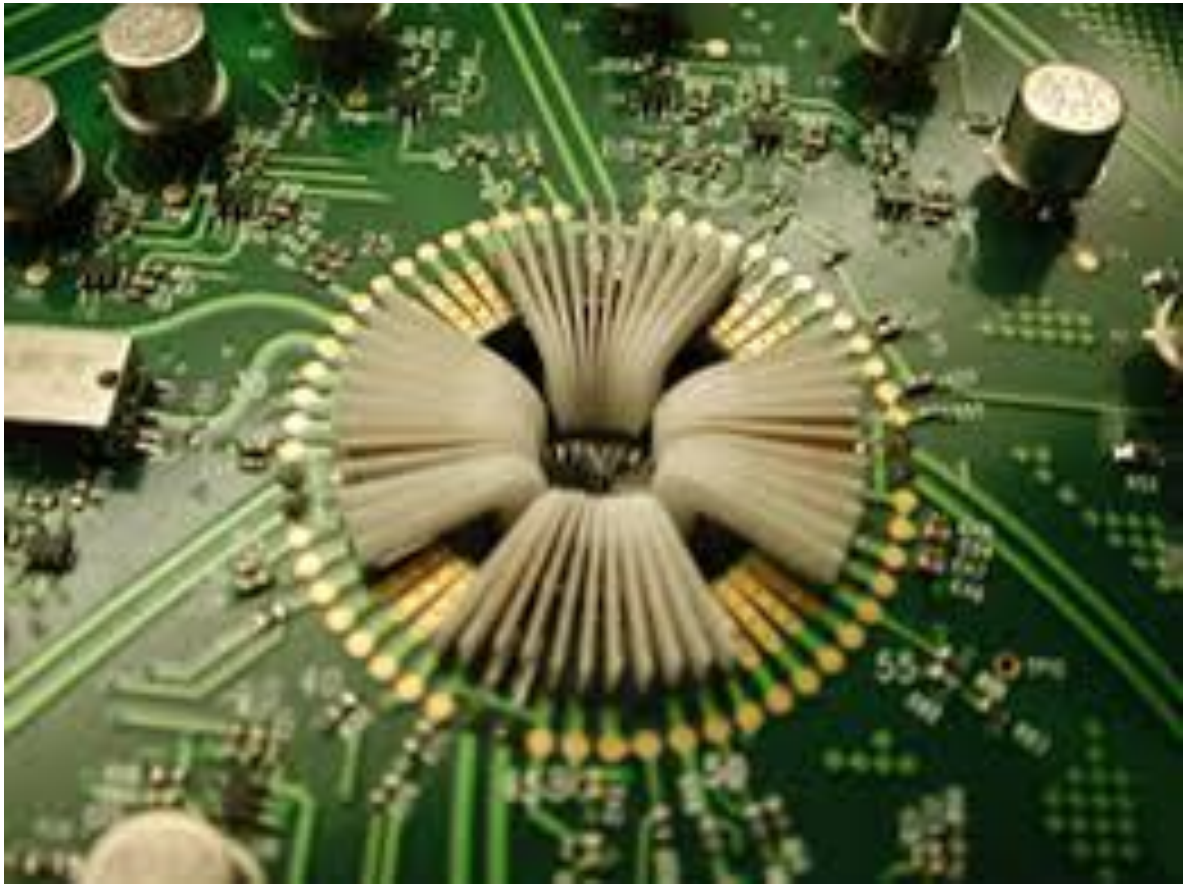


Photos from www postings and Google image search

Bench Test Environment

Photo courtesy of Texas Instruments

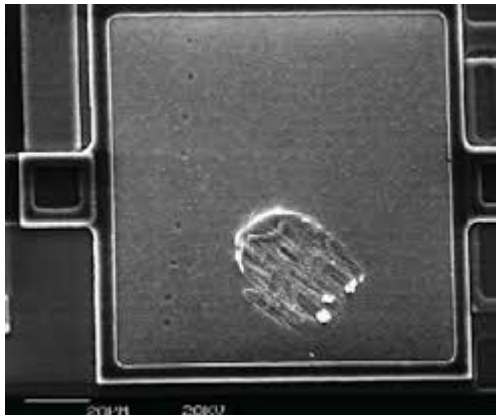
Probe Test



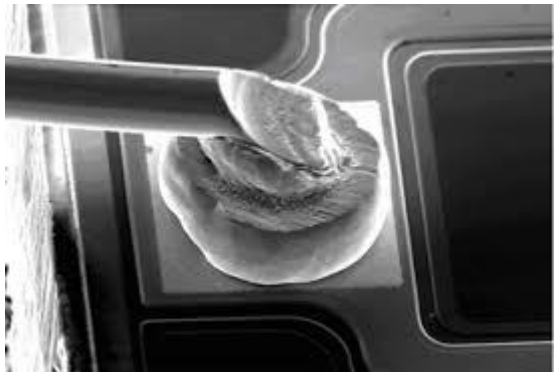
Probes on section of probe card

Photos from www postings and Google image search

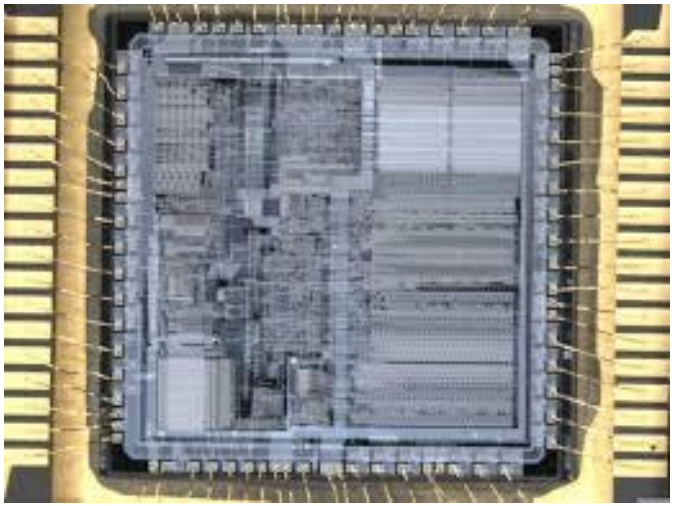
Probe Test



Pad showing probe marks



Pad showing bonding wire



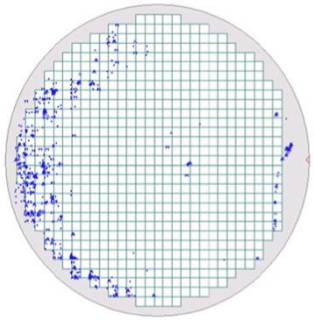
Die showing wire bonds to package cavity

Photos from www postings and Google image search

Probe Test

Production probe test facility

Goal to Identify
defective die on wafer



Photos from www postings and Google image search

Final Test

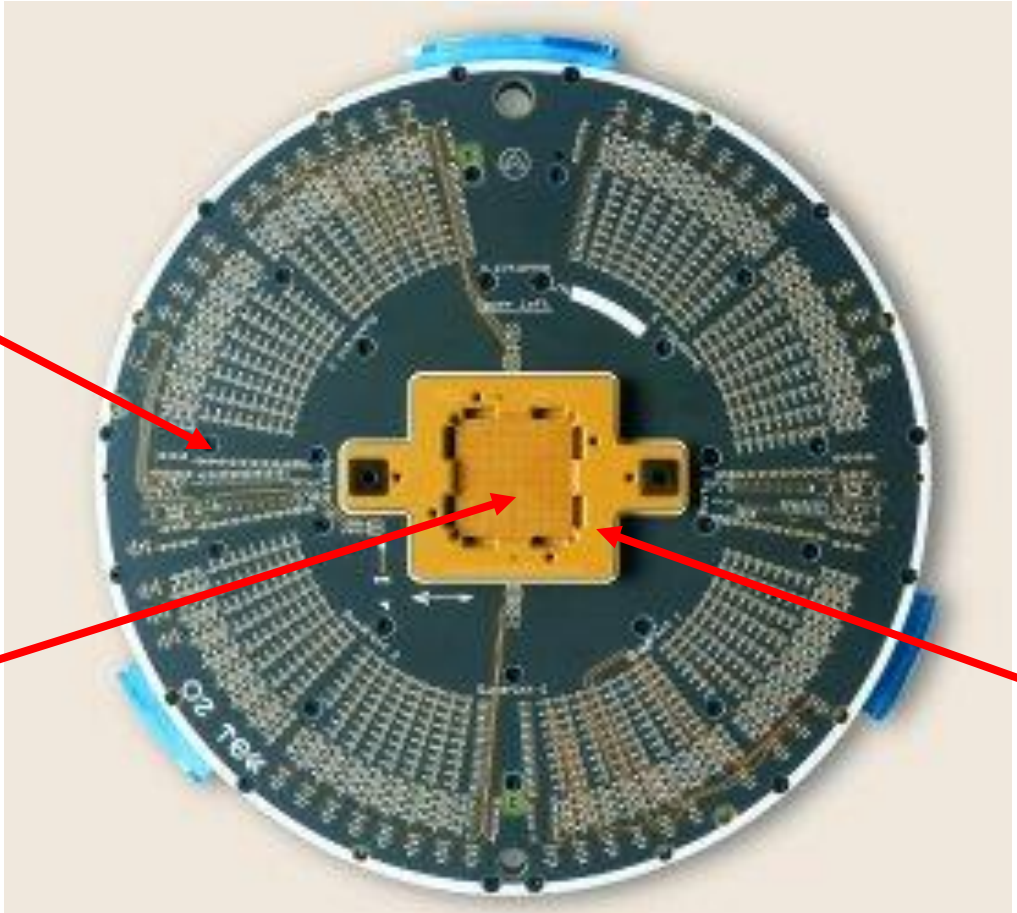
Typical ATE System (less handler)

Automated Test Equipment (ATE)

Device Interface Board - DIB

(Load Board)

DIB



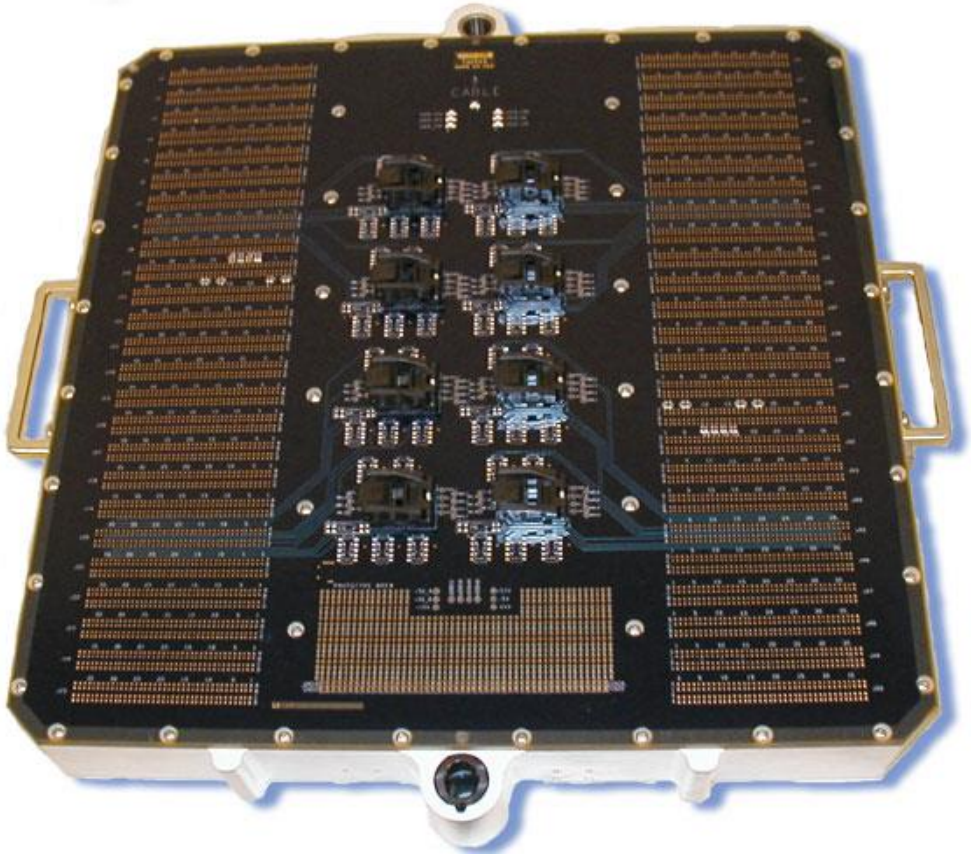
Cavity
(for DUT)

Socket
(Contactor)

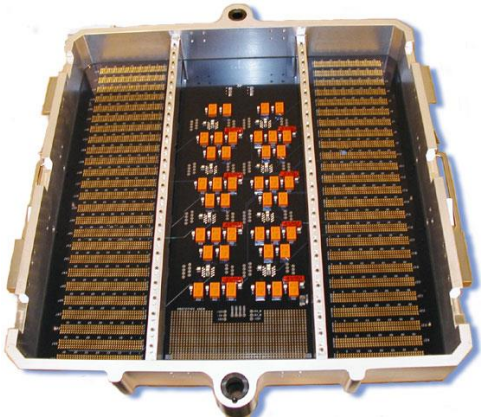
DIBs Vary Considerably from one ATE Platform to another and are often personalized for a particular DUT

Octal Site DIB

Flex Octal (Teradyne)



Top



Bottom

Final Test

Typical ATE Configuration

Handler

Tester

Test Head

Atlas (SSI Robotics)

Basic Semiconductor Processes

MOS (Metal Oxide Semiconductor)

1. NMOS — n-ch
2. PMOS — p-ch
3. CMOS — n-ch & p-ch
   - Basic Device: MOSFET
   - Niche Device: MESFET
   - Other Devices: Diode
     BJT
     Resistors
     Capacitors
     Schottky Diode

Basic Semiconductor Processes

Bipolar

1. T^2L
2. ECL
3. I^2L
4. Linear ICs
   - Basic Device: BJT (Bipolar Junction Transistor)
   - Niche Devices: HBJT (Heterojunction Bipolar Transistor)
     HBT
   - Other Devices: Diode
     Resistor
     Capacitor
     Schottky Diode
     JFET (Junction Field Effect Transistor)

Basic Semiconductor Processes

Other Processes

- Thin and Thick Film Processes
  - Basic Device: Resistor
- BiMOS or BiCMOS
  - Combines both MOS & Bipolar Processes
  - Basic Devices: MOSFET & BJT
- SiGe
  - BJT with HBT implementation
- SiGe / MOS
  - Combines HBT & MOSFET technology
- SOI / SOS (Silicon on Insulator / Silicon on Sapphire)
- Twin-Well & Twin Tub CMOS
  - Very similar to basic CMOS but more optimal transistor char.

Devices in Semiconductor Processes

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (decent in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel
- Standard Bipolar Process
  - BJT
    - npn
    - pnp
  - JFET
    - n-channel
    - p-channel
  - Diodes
  - Resistors
  - Capacitors

- Niche Devices
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET
  - HBT
  - Schottky Diode (not Shockley)
  - MEM Devices
  - TRIAC/SCR
  - ….

Basic Devices

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel
- Niche Devices
  - Photodetectors
  - MESFET
  - Schottky Diode (not Shockley)
  - MEM Devices
  - Triac/SCR
  - ….

Primary Consideration in This Course

Some Consideration in This Course

Stay Safe and Stay Healthy !

End of Lecture 12